DATE: August 16, 2010 **PAGES (+COVER):** 4

FROM: Patrick D. Reed	**TO:** Ben C. Wang
PHONE: 509-944-4752	**PHONE:** 571-270-1240
FAX #: 509-323-8979	**FAX #:** 571-270-2240

lee&hayes

RE: 10/816,558 -Interview Request From

COMMENTS:

Hello Examiner Wang,

Please confirm receipt of fax and acceptance of interview.

I look forward to working with you on this matter.

Regards,

Patrick

Thanks

SPOKANE 509•324•9256 / fax 509•323•8979 SEATTLE 206•315•4001 / fax 206•315•4004 AUSTIN 512•505•8162 / fax 509•944•4695

Attorney Docket MS1 - 4217US

PTOL-413A (07-09)
Approved for use through 07/31/2012. OMB 0651-0031
U.S. Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE

Applicant Initiated Interview Request Form

Application No.: 10/816,558 First Named Applicant: Lucius Gregory Meredith

Examiner: Ben C. Wang Art Unit: 2192 Status of Application: Non-Final

Tentative Participants:

(1) Ben C. Wang (2) Patrick D. Reed

(3) _____ (4) _____

Proposed Date of Interview: Thurs, August 19, 2010 **Proposed Time:** 1:30pm EDT **AM/PM**

Type of Interview Requested:

(1) ☑ **Telephonic** (2) ☐ **Personal** (3) ☐ **Video Conference**

Exhibit To Be Shown or Demonstrated: ☐ **YES** ☐ **NO**

If yes, provide brief description: _____

Issues To Be Discussed

Issues (Rej., Obj., etc)	Claims/ Fig. #s	Prior Art	Discussed	Agreed	Not Agreed
(1) 103 Rej.	6, 42	Leach, Meredith	☐	☐	☐
(2)			☐	☐	☐
(3)			☐	☐	☐
(4)			☐	☐	☐

☐ Continuation Sheet Attached

Brief Description of Argument to be Presented:

1) Distinguishing the claims from the cited references in light of the proposed amendments.

An interview was conducted on the above-identified application on _____ .

NOTE: This form should be completed by applicant and submitted to the examiner in advance of the interview (see MPEP § 713.01).

This application will not be delayed from issue because of applicant's failure to submit a written record of this interview. Therefore, applicant is advised to file a statement of the substance of this interview (37 CFR 1.133(b)) as soon as possible.

P-D Reed

Applicant/Applicant's Representative Signature

Patrick D. Reed

Typed/Printed Name of Applicant or Representative

61227

Registration Number, if applicable

Examiner/SPE Signature

Attorney Docket MS1 - 4217US

Unofficial Communication – For Discussion Purposes Only
Application No. 10/816,558

6. (Proposed Amendments) A microprocessor for executing instructions, comprising:

a timing and control unit ~~for retrieving~~ configured to:

retrieve an instruction to compose a plurality of processes running in parallel from a memory, the instruction being expressed in a reflective process algebra, the reflective process algebra being arranged to represent a name as a literalization of a process and a process as a deliteralization of a name,

~~decoding~~ decode the instruction,

~~fetching~~ fetch data connected with the instruction, the data comprising at least a first name that is a literalization of a first process and a second name that is a literalization of a second process, the first name and the second name being obtained using the reflective process algebra, and

~~saving the~~ literalize a result of a composing, including saving the result of the composing ~~the data including names obtained by literalizing processes in a reflective process algebra~~; and

an arithmetic and logic unit ~~for performing an operation specified by the instruction~~ configured to perform the composing of the plurality of processes running in parallel, the composing including deliteralizing the first name and the second name ~~the instruction being expressed in a reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names~~.

45. (Proposed Amendments) An array of microprocessors for executing instructions, comprising:

at least one microprocessor that includes one or more components that are synchronized based on a program compiler configured to compile a program written in a reflective process algebra:

a timing and control unit for retrieving an instruction from memory, decoding the instruction, fetching data connected with the instruction, and saving [[the]] a result, the data including names obtained by literalizing processes in the reflective process algebra; and

an arithmetic and logic unit for performing an operation specified by the instruction, the instruction being expressed in [[a]] the reflective process algebra, the reflective process algebra being capable of representing names as literalization of processes and processes as deliteralization of names.